IN THE SPECIFICATION:

Please replace paragraph [0046] with the following amended paragraph:

-- In FIGs. 6 to 8, the gate line 121 is formed on a substrate 110, and the gate insulation layer 130 is formed on the substrate 110 and covers the gate line 121. An intrinsic semiconductor layer 141 may be formed on the gate insulation layer 130, and an extrinsic semiconductor layer 151 may be formed on the intrinsic semiconductor layer 141. The intrinsic semiconductor layer 141 may be formed of pure amorphous silicon and the extrinsic semiconductor layer 151 may be formed of doped amorphous silicon. The data line 161 that is perpendicular to the gate line 121 may be formed on the extrinsic semiconductor layer 151, and the dummy metal layers 166 may be formed on both sides of the data line 161 and located above the gate line 121. A passivation layer 171 may be formed on the data line 161 and on the dummy metal layers 166 and may have the same shape as the data line 161 except for a portion at a crossover point of the gate line 121 and data line 161. The passivation layer 171 has a first width W1 disposed along directions of the data and gate lines 121 and 161 and a second width W2 larger than the first width W1 at the crossover point to cover not only the data line 161 but also the dummy metal layers 166.--

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